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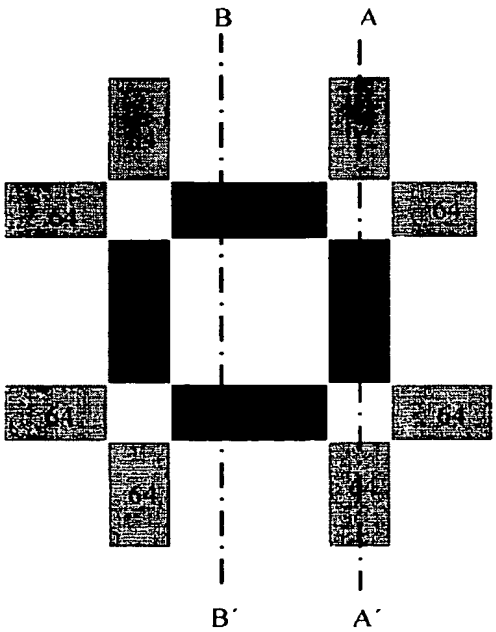

(57) Abstract: A trench MOSFET device and method of making the same. The trench MOSFET device comprises: a) semiconductor substrate of first conductivity type; b) an epitaxial region of first conductivity type provided within a lower portion of a semiconductor epitaxial layer disposed on the substrate, wherein the epitaxial region of first conductivity type has a lower majority carrier concentration than the substrate; c) a region of second conductivity type provided within an upper portion of the semiconductor epitaxial layer; d) a plurality of trench segments in an upper surface of the semiconductor epitaxial layer, wherein: i) the plurality of trench segments extend through the region of second conductivity type and into the epitaxial region of first conductivity type, ii) each trench segment is at least partially separated from an adjacent trench segment by a terminating region of the semiconductor epitaxial layer, and iii) the trench segments define a plurality of polygonal body regions within the region of second conductivity type; e) a first insulating layer at least partially lining each trench segment; f) a plurality of first conductive regions within the trench segments adjacent to the first insulating layer, wherein each of the first conductive regions is connected to an adjacent first conductive region by a connecting conductive region that bridges at least one of the terminating regions; and g) a plurality of source regions of the first conductivity type positioned within upper portions of the polygonal body regions and adjacent the trench segments. The body regions are preferably either rectangular body regions defined by four trench segments or hexagonal body regions defined by six trench segments.

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TRENCH MOSFET WITH STRUCTURE HAVING LOW GATE CHARGE

FIELD OF THE INVENTION

The present invention relates to microelectronic circuits, and more particularly to trench MOSFET devices.

BACKGROUND OF THE INVENTION

Metal oxide semiconductor field effect transistor (MOSFET) devices that use trench gates provide low turn-on resistance. In such trench MOSFET devices, the channels are arranged in a vertical manner, instead of horizontally as in most planar configurations. FIG. 1 shows a partial cross-sectional view of a conventional trenched gate MOSFET device 2. The MOSFET device includes a trench 4 filled with conductive material 6 separated from the silicon regions 8 by a thin layer of insulating material 10. A body region 12 is diffused in an epitaxial layer 18, and a source region 14 is in turn diffused in the body region 12. Due to the use of these two diffusion steps, a transistor of this type is frequently referred to as a double-diffused metal oxide semiconductor field effect transistor with trench gating or, in brief, a "trench DMOS".

As arranged, the conductive and insulating materials 6 and 10 in the trench 4 form the gate 15 and gate oxide layer 16, respectively, of the trench DMOS. In addition, the depth L measured from the source 14 to the epitaxial layer 18 constitutes the channel length L of the trench DMOS device. The epitaxial layer 18 is a part of the drain 20 of the trench DMOS device.

When a potential difference is applied across the body 12 and the gate 15, charges are capacitively induced within the body region 12 adjacent to the gate oxide layer 16, resulting in the formation of the channel 21 of the trench DMOS

device. When another potential difference is applied across the source 14 and the drain 20, a current flows from the source 14 to the drain 20 through the channel 21, and the trench DMOS device is said to be in the power-on state.

Examples of trench DMOS transistors are disclosed in U.S. Patent Nos. 5,907,776, 5,072,266, 5,541,425, and 5,866,931, the entire disclosures of which are hereby incorporated by reference.

A typical discrete trench MOSFET circuit includes two or more individual trench MOSFET transistor cells which are fabricated in parallel. The individual trench MOSFET transistor cells share a common drain contact, while their sources are all shorted together with metal and their gates are shorted together by polysilicon. Thus, even though the discrete trench MOSFET circuit is constructed from a matrix of smaller transistors, it behaves as if it were a single large transistor.

Unit cell configurations of trench MOSFET circuits can take various forms. Figures 2A and 2B illustrate two trench configurations commonly employed in the prior art. In contrast to Figure 1, which represents a partial cross-sectional side (or elevation) view of a single trench section within a MOSFET circuit, Figures 2A and 2B represent partial overhead (or plan) views of two trench networks. In particular, Figure 2A illustrates a partial section of a trench network 4 in which the trenches collectively form a series of hexagonal unit cells (an expanded view would show the cells to be in a honeycomb pattern). Figure 2B illustrates a partial section of a trench network 4 in which the trenches form a series of square unit cells (an expanded view would show the cells to be arranged in the fashion of squares in a grid). Figure 2B can be thought of as being formed by the intersection of two sets of parallel trench lines. All trench areas (i.e., all dark regions) of Figures 2A and 2B are of essentially the same depth within the trench network.

Demand persists for trench DMOS devices having ever-lower on-resistance. The simplest way to reduce on-resistance is to increase cell density. Unfortunately, the gate charges associated with trench DMOS devices increase when cell density is increased.

Hence, efforts to provide low on-resistance in trench DMOS devices by increasing cell density are presently frustrated by detrimental changes that simultaneously occur, for example, in the gate charges associated with those devices.

SUMMARY OF THE INVENTION

The above and other obstacles in the prior art are addressed by the trench MOSFET devices and methods of the present invention.

According to an embodiment of the invention, a trench MOSFET device is provided. The trench MOSFET device comprises:

a) a semiconductor substrate of first conductivity type;

b) an epitaxial region of first conductivity type provided within a lower portion of a semiconductor epitaxial layer disposed on the substrate, wherein the epitaxial region of first conductivity type has a lower majority carrier concentration than the substrate;

c) a region of second conductivity type provided within an upper portion of the semiconductor epitaxial layer;

d) a plurality of trench segments in an upper surface of the semiconductor epitaxial layer, wherein: i) the plurality of trench segments extend through the region of second conductivity type and into the epitaxial region of first conductivity type, ii) each trench segment is at least partially separated from an adjacent trench segment by a terminating region of the semiconductor epitaxial layer, and iii) the trench segments define a plurality of polygonal body regions within the region of second conductivity type;

e) a first insulating layer at least partially lining each trench segment;

f) a plurality of first conductive regions within the trench segments adjacent to the first insulating layer, wherein each of the first conductive regions is connected to an adjacent first conductive region by a connecting conductive region that bridges at least one of the terminating regions; and

g) a plurality of source regions of the first conductivity type positioned within upper portions of the polygonal body regions and adjacent the trench segments.

The body regions are preferably either rectangular body regions defined by four trench segments or hexagonal body regions defined by six trench segments.

In some preferred embodiments: i) the trench MOSFET device is a silicon device, ii) the first conductivity type is n-type conductivity and the second conductivity type is p-type conductivity, and more preferably the substrate is an N+ substrate, the epitaxial region of first conductivity type is an N region, the body regions comprise P regions, and the source regions are N+ regions, iii) the first insulating layers are oxide layers, iv) the first conductive regions and the connecting conductive regions are polysilicon regions and/or v) a drain electrode is disposed on a surface of the substrate and a source electrode is disposed on at least a portion of the source regions.

According to another embodiment of the invention, a method of forming a trench MOSFET device is provided. The method comprises:

a) providing semiconductor substrate of first conductivity type;
b) forming a semiconductor epitaxial layer over the semiconductor substrate, the epitaxial layer being of the first conductivity type and having a lower majority carrier concentration than the substrate;
c) forming a region of second conductivity type within an upper portion of the semiconductor epitaxial layer (for example, by a method comprising implanting and diffusing a dopant into the epitaxial layer), such that an epitaxial region of first conductivity type remains within a lower portion the semiconductor epitaxial layer;
d) forming a plurality of trench segments in an upper surface of the epitaxial layer (for example, by a method comprising forming a patterned masking layer over the epitaxial layer and etching the trenches through the masking layer), wherein: (i) the trench segments extend through the region of second conductivity type and into the epitaxial region of first conductivity type, (ii) each trench segment

is at least partially separated from an adjacent trench segment by a terminating region of the semiconductor epitaxial layer, and (iii) the trench segments define a plurality of polygonal body regions within the region of second conductivity type;

e) forming a first insulating layer within each trench segment;

f) forming a plurality of first conductive regions within the trench segments adjacent to the first insulating layer;

g) forming a plurality of connecting conductive regions, wherein each of the connecting conductive regions bridges at least one of the terminating regions and connects one of the first conductive regions to an adjacent first conductive region; and

h) forming a plurality of source regions of the first conductivity type within upper portions of the polygonal body regions and adjacent the trench segments.

The first insulating layer is preferably an oxide layer and is formed via dry oxidation.

The step of forming the source regions preferably comprises forming a patterned masking layer and implanting and diffusing a dopant into upper portions of the polygonal body regions.

The first conductive regions and the connecting conductive regions are preferably polysilicon regions, and are preferably formed simultaneously. More preferably, the first conductive regions and the connecting conductive regions are formed by a method comprising depositing a layer of polycrystalline silicon, placing a patterned masking layer over the polycrystalline silicon, and etching the polycrystalline silicon layer though the patterned mask.

One advantage of the present invention is that a trench MOSFET device with increased cell density, and hence lower on-resistance, is provided, while minimizing increases in gate charge.

Another advantage of the present invention is that such a device can be made with relative simplicity.

These and other embodiments and advantages of the present invention will become immediately apparent to those of ordinary skill in the art upon review of the Detailed Description and Claims to follow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partial cross-sectional view of a conventional trench DMOS device.

FIGS. 2A and 2B illustrate partial overhead (or plan) views of trench configurations associated with DMOS devices having hexagonal and square unit cells, respectively.

Figure 3 shows a partial overhead (or plan) view of a MOSFET trench network like that shown in Figure 2, in which areas of substantial and insubstantial current flow are shown.

Figure 4A is a partial cross-sectional view of a trench MOSFET device having trench structure like that of Figure 3. The view is taken along a plane analogous to that represented by line A-A′ of Figure 3.

Figure 4B is a partial cross-sectional view of a trench MOSFET device having trench structure like that of Figure 3. The view of Figure 4B is taken along a plane analogous to that represented by line B-B′ of Figure 3.

Figure 5 is a plot of % inactive area vs. cell density for a trench MOSFET device having a trench structure like that of Figure 3.

Figure 6 is a partial overhead (or plan) view of a trench configuration of a MOSFET circuit in accordance with one embodiment of the invention.

Figures 7A is a partial cross-sectional view of a MOSFET device having the trench structure of Figure 6. The view is taken along a plane analogous to that represented by line A-A′ of Figure 6.

Figures 7B is a partial cross-sectional view of a MOSFET device having the trench structure of Figure 6. The view is taken along a plane analogous to that represented by line B-B′ of Figure 6.

Figures 8A to 8D illustrate partial plan views of various trench designs by which trench segments and trench lines can be used to form square cells of a MOSFET device.

Figures 9A-9E and 10A-10E illustrate a method for manufacturing a trench MOSFET of the present invention according to an embodiment of the invention. Figures 9A-9E are taken along a view like that of Figure 7A. Figures 10A-10E are taken along a view like that of Figure 7B.

Figure 11 is a partial cross-sectional view of a trench MOSFET of the prior art.

DETAILED DESCRIPTION OF THE INVENTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the present invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein.

Figure 3 shows a trench pattern like that of Figure 2B. In this figure, two sets of parallel trench lines intersect to form a square unit cell 70. The dark areas of the trench lines (designated 54b) correspond to portions of the trench where there is a substantial source-to-drain current flow in the power-on state (referred to herein as the "active trench sections"), while the light areas (designated 54c) correspond to portions of the trench lines where there is no substantial source-to-drain current flow in the power-on state (referred to herein as the "inactive trench sections"). These inactive trench sections 54c correspond in location to positions where the trench lines intersect.

The current flow can be seen more clearly in Figure 4A, which is a cross-sectional view of a trench MOSFET device having trench structure like that of Figure 3. The view is taken along a plane analogous to that represented by line A-A′ of Figure 3. This figure shows an N+ substrate 50, with N epitaxial layer 52 and a gate trench (composed active 54b and inactive regions 54c), lined with an

insulating material, typically an oxide (not shown), and filled with a conductive material such as polysilicon 58. Current flow from the drain to the surface of active trench regions 54b is illustrated by the arrows in Figure 4A. Inactive trench regions 54c are essentially devoid of such current, and hence there are no arrows in these regions.

The view of Figure 4B is taken along a plane analogous to that represented by line B-B′ of Figure 3. Illustrated in this figure are P-body regions 56 (the sources of the device are not shown), as well as an N+ substrate 50, N epitaxial layer 52 and polysilicon regions 58 (the insulating material is not shown) within the trenches. As in Figure 4A, current flow from the drain to the surface of the active trench regions 54a is illustrated by arrows. Because section B-B′ does not encompass any area where trenches overlap, no inactive trench regions 54c are encompassed by section B-B′.

As will be immediately appreciated by those of ordinary skill in the art, as the cell density of Figure 3 increases (i.e., as the dimensions of the trench segments in Figure 3 decrease), the percentage of the inactive area associated with a given closed cell also increases. More specifically, as shown in Figure 5, as the cell density increases from 49 million cells per square inch to 290 million cells per square inch, the relative area of the trenches that is inactive increases from about 10% of the total trench area to about 45% of the total trench area. Although the inactive area does not contribute to current flow, it does contribute to the gate charge, and in particular the charge between the gate and drain (Qgd). As a result, the relative Qgd contribution from the inactive area also increases as cell density increases.

To overcome this problem, the present inventors propose a novel trench structure, which is composed of discrete trench segments, rather than a continuous trench network.

Turning now to Figure 6, a partial overhead (or plan) view of a trench configuration of a MOSFET circuit is shown in accordance with one embodiment of the invention. This figure shows twelve trench segments 64. Unlike Figure 3

above, where trench lines 54 intersect to form a continuous trench network, trench segments 64 do not substantially intersect and hence represent a series of discrete trenches.

This feature can be better seen in Figures 7A and 7B. Figure 7A is a cross-sectional view of a device having a trench structure like that of Figure 6. The view is taken along a plane analogous to that represented by line A-A′ of Figure 6. This figure shows an N+ substrate 60, with N epitaxial layer 62, P-body regions 66, and trench segments, which are lined with oxide (not shown) and filled with polysilicon 68. Besides filling trench segments, the polysilicon 68 also covers portions of the P-body regions 66. Current flow from the drain to the surface of the gate trench segments is illustrated by the arrows in Figure 7A. As can bee seen in this figure, all trench segments are active trench segments 64b. Although inactive areas remain where current flow is absent, these areas are associated with the P body regions 66, rather than the trench segments. In contrast, the inactive area 54c in Figure 4A above are associated with the trenches. This modification is advantageous in that the gate charges associated with inactive trench sections 54c of Figure 4A are no longer present.

The view of Figure 7B is taken along a plane analogous to that represented by line B-B′ of Figure 6. As in Figure 7A, the N+ substrate 60, N epitaxial layer 62, trench segments 64, P-body regions 66 and polysilicon regions 68 are illustrated. Arrows illustrate current flow from the drain to the surface of the trench segments, which are active trench segments 64b. The view of Figure 7B does not differ substantially from the view of Figure 4B.

The embodiment of the present invention immediately above is directed to a MOSFET structure having cells surrounded on four sides by trench segments (square cell structure). As used herein a "trench segment" is a short trench forming a side of a polygonal cell. Rather than extending substantially beyond the length of a cell side, a trench segment is at least partially terminated at its ends by semiconductor regions that are proximate the corners of the polygonal cell. Figures 8A to 8D illustrate partial plan views of various trench designs by which trench

segments 64s (Figures 8A-8C) and trench lines 64t (Figures 8D) can be used to form square cells 70 of a MOSFET device. Figure 8A illustrates the case where trench segments 64s are completely terminated by a semiconductor region 66+ (which, as seen in Figure 7A, typically corresponds to the p-body region 66 and a portion of the N-epitaxial region 62 as well). In Figure 8B, adjacent trench segments 64s just meet one another, still resulting in essentially complete termination by the semiconductor region 66+. In Figure 8C, the trench segments 64s are partially terminated by the semiconductor region 66+.

Finally, Figure 8D illustrates the configuration of the prior art. The semiconductor cells 70 are surrounded on four sides by trench lines 64t that extend beyond each cell 70 to form sides of other cells. At the corners of the square cells 70 each trench 64t is essentially unobstructed by a semiconductor region.

A method for manufacturing the trench MOSFET of the present invention will now be described in connection with Figures 9A-9E, which are taken along a view like that of Figure 7A, and in connection with Figures 10A-10E, which are taken along a view like that of Figure 7B. As noted above, the view of Figure 7B (which is analogous to Figure 10E) is substantially like that of the prior art. This structure can further include termination features that are well known in the art.

Referring now to these figures, in this specific example, an N doped epitaxial layer 202 is initially grown on an N+ doped substrate 200. For example, epitaxial layer 202 can be 6.0 microns thick and have an n-type doping concentration $3.4 \times 10^{16}\ cm^{-3}$, while N+ doped substrate 200 can be 250 microns thick and have an n-type doping concentration of $5 \times 10^{19}\ cm^{-3}$. A P-type layer 204 is then formed in the epitaxial layer 202 by implantation and diffusion. For example the epitaxial layer 202 may be implanted with boron at 40 keV with a dosage of $6 \times 10^{13}\ cm^{-2}$, followed by diffusion to a depth of 1.8 microns 1150° C. The resulting structure is shown in Figures 9A and 10A.

A mask oxide layer is then deposited, for example by chemical vapor deposition, and patterned using a trench mask (not shown). Trench segments 201 are etched through apertures in the patterned mask oxide layer 203, typically by

reactive ion etching. Trench depths in this example are about 2.0 μm. Discrete P-regions 204, 204′ are established as a result of this trench-forming step. Some of these P-regions 204 correspond to the body regions within the device cell. Others of these P-regions 204′ act to terminate the trench segments and do not constitute part of a device cell (as seen below, P-regions 204' are not provided with source regions). The resulting structure is shown in Figures 9B and 10B.

The patterned mask oxide layer 203 is then removed and an oxide layer 210 is grown in its place, typically by dry oxidation at 950 to 1050 °C. Oxide layer 210 ultimately forms the gate oxide for the finished device. A thickness in the range of 500 to 700 Angstroms is typical for oxide layer 210. The surface of the structure is then covered, and the trenches are filled, with a polysilicon layer, typically using CVD. The polysilicon is typically doped N-type to reduce its resistivity, generally on order of 20 Ω/sq. N-type doping can be carried out, for example, during CVD with phosphorous chloride or by implantation with arsenic or phosphorous.

The polysilicon layer is then etched, for example, by reactive ion etching. The polysilicon layer within the trench segments is slightly over-etched due to etching uniformity concerns, and the thus-formed polysilicon gate regions 211g typically have top surfaces that are 0.1 to 0.2 microns below the adjacent surface of the epitaxial layer 204 (see, e.g., Figure 10C). A mask is used during etching to ensure that polysilicon regions 211b are established over regions 204′, allowing the polysilicon gate regions 211g to be in electrical contact with one another. Typically, a mask is used to preserve polysilicon in the gate runner region, so an additional mask step is not required.

The oxide layer 210 is then wet etched to a thickness of 100 Angstroms to form an implant oxide. The implant oxide avoids implant-channeling effects, implant damage, and heavy metal contamination during subsequent formation of source regions. A patterned masking layer 213 is then provided over portions of the P-regions 204. The resulting cross-sectional views of this structure are shown in Figures 9C and 10C.

Source regions 212 are typically formed within upper portions of the P-body regions 204 via an implantation and diffusion process. For example, the source regions 212 may be implanted with arsenic at a dosage of 1×10^{16} cm^{-2} and diffused to a depth of 0.4 microns at a temperature of 950°C.

A BPSG (borophosphosilicate glass) layer is then be formed over the entire structure, for example, by PECVD, and provided with a patterned photoresist layer (not shown). The structure is etched, typically by reactive ion etching, to remove the BPSG and oxide layers 210 over at least a portion of each source region 212. The resulting cross-sectional views of this structure are shown in Figures 9D and 10D. (In this embodiment, boron P+ regions 215 are formed between the source regions by P+ implant after contact is opened.)

The photoresist layer is then removed and the structure provided with a metal contact layer 218 (aluminum in this example), which contacts the source regions 214 and acts as a source electrode. (In this embodiment, boron is implanted to form the P+ regions 215 before the metal is deposited.) The resulting cross-sectional views of this structure are shown in Figures 9E and 10E. In the same step, a separate metal contact (not shown) is connected to the gate runner, which is located outside the cells. Another metal contact (also not shown) is typically provided in connection with substrate 200, which acts as a drain electrode.

As noted above, when examined along line B-B′, the structure of the present invention (see Figure 10E) looks essentially the same a prior art structures. When examined along line A-A′, however, the structure of the present invention (Figure 9E) is radically different than the prior art. Figure 11 is representative of such a prior art structure. The prior art structure of Figure 11 contains a single trench line along line A-A′ that is lined with oxide 210 and filled with polysilicon 211g. In contrast, the device of Figure 9E contains numerous trench segments that are lined with oxide 210 and filled with polysilicon 211g. These trench segments terminate at semiconductor regions 204′ that were not etched during processing. Polysilicon regions 211b are established over regions 204′ to contact polysilicon gate regions

211g with one another. Since no gate structure is established in these regions 204', gate capacitance is eliminated.

Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention. For example, the method of the present invention may be used to form a structure in which the conductivities of the various semiconductor regions are reversed from those described herein.

What is claimed is:

1. A trench MOSFET device comprising:

a semiconductor substrate of first conductivity type;

an epitaxial region of first conductivity type provided within a lower portion of a semiconductor epitaxial layer disposed on said substrate, said epitaxial region of first conductivity type having a lower majority carrier concentration than said substrate;

a region of second conductivity type provided within an upper portion of said semiconductor epitaxial layer;

a plurality of trench segments in an upper surface of said semiconductor epitaxial layer, said plurality of trench segments extending through the region of second conductivity type and into said epitaxial region of first conductivity type, each said trench segment being at least partially separated from an adjacent trench segment by a terminating region of said semiconductor epitaxial layer, said trench segments defining a plurality of polygonal body regions within said region of second conductivity type;

a first insulating layer at least partially lining each said trench segment;

a plurality of first conductive regions within said trench segments adjacent to the first insulating layer, each said first conductive regions being connected to an adjacent first conductive region by a connecting conductive region that bridges at least one of said terminating regions; and

a plurality of source regions of said first conductivity type positioned within upper portions of said polygonal body regions and adjacent said trench segments.

2. The trench MOSFET device of claim 1, wherein said plurality of body regions are rectangular body regions defined by four trench segments.

3. The trench MOSFET device of claim 1, wherein a said plurality of body regions are hexagonal body regions defined by six trench segments.

4. The trench MOSFET device of claim 1, wherein said trench MOSFET device is a silicon device.

5. The trench MOSFET device of claim 1, wherein the first conductivity type is n-type conductivity and the second conductivity type is p-type conductivity.

6. The trench MOSFET device of claim 1, further comprising a drain electrode disposed on a surface of the substrate and a source electrode disposed on at least a portion of the source regions.

7. The trench MOSFET device of claim 1, wherein said first insulating layer is an oxide layer.

8. The trench MOSFET device of claim 1, wherein said first conductive regions and said connecting conductive regions are polysilicon regions.

9. The trench MOSFET device of claim 5, wherein said substrate is an N+ substrate, said epitaxial region of first conductivity type is an N region, said body regions comprise P regions, and said source regions are N+ regions.

10. A method of forming a trench MOSFET device comprising:

providing semiconductor substrate of first conductivity type;

forming a semiconductor epitaxial layer over said semiconductor substrate, said epitaxial layer being of said first conductivity type and having a lower majority carrier concentration than said substrate;

forming a region of second conductivity type within an upper portion of said semiconductor epitaxial layer, such that an epitaxial region of first conductivity type remains within a lower portion said semiconductor epitaxial layer;

forming a plurality of trench segments in an upper surface of said epitaxial layer, (i) said trench segments extending through the region of second conductivity type and into said epitaxial region of first conductivity type, (ii) each said trench segment being at least partially separated from an adjacent trench segment by a terminating region of said semiconductor epitaxial layer, and (iii) said trench segments defining a plurality of polygonal body regions within said region of second conductivity type;

forming a first insulating layer lining each said trench segment;

forming a plurality of first conductive regions within said trench segments adjacent to the first insulating layer;

forming a plurality of connecting conductive regions, each of said connecting conductive regions bridging at least one of said terminating regions and connecting one of said first conductive regions to an adjacent first conductive region; and

forming a plurality of source regions of said first conductivity type within upper portions of said polygonal body regions and adjacent said trench segments.

11. The method of claim 10, wherein said polygonal body regions are rectangular body regions, each defined by four trench segments.

12. The method of claim 10, wherein a said polygonal body regions are hexagonal body regions, each defined by six trench segments.

13. The method of claim 10, wherein said MOSFET device is a silicon device.

14. The method of claim 10, wherein said step of forming said region of second conductivity type comprising implanting and diffusing a dopant into the epitaxial layer.

15. The method of claim 10, wherein the step of forming said trench segments comprises forming a patterned masking layer over the epitaxial layer and etching said trenches through said masking layer.

16. The method of claim 10, wherein said first insulating layer is an oxide layer.

17. The method of claim 16, wherein the oxide layer is formed via dry oxidation.

18. The method of claim 10, wherein the first conductive regions and the connecting conductive regions are polysilicon regions.

19. The method of claim 18, wherein the plurality of first conductive regions and the plurality of connecting conductive regions are formed simultaneously.

20. The method of claim 19, wherein said plurality of first conductive regions and said plurality of connecting conductive regions are formed by a method comprising depositing a layer of polycrystalline silicon, placing a patterned masking layer over said polycrystalline silicon, and etching the polycrystalline silicon layer though said patterned mask.

21. The method of claim 14, wherein the step of forming the source regions comprises forming a patterned masking layer and implanting and diffusing a dopant into upper portions of the polygonal body regions.

22. The method of claim 16, wherein said first conductivity type is N-type conductivity, and wherein said second conductivity type is P-type conductivity.

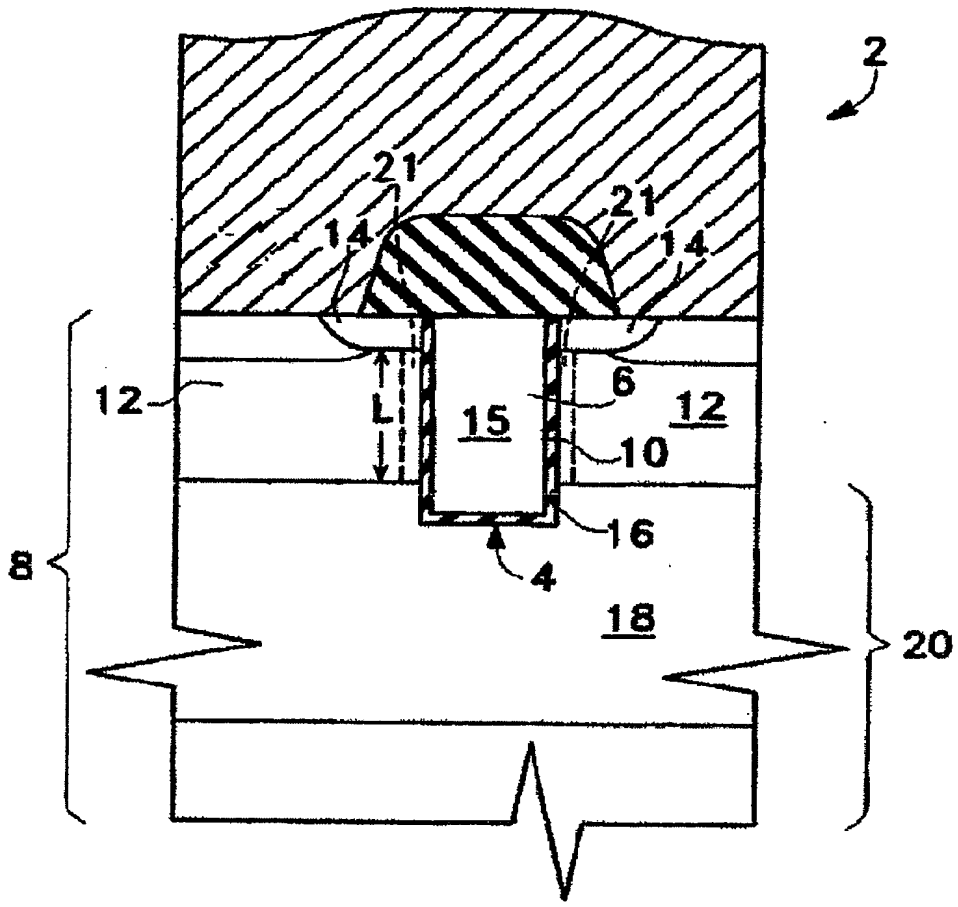

FIG. 1 (Prior Art)

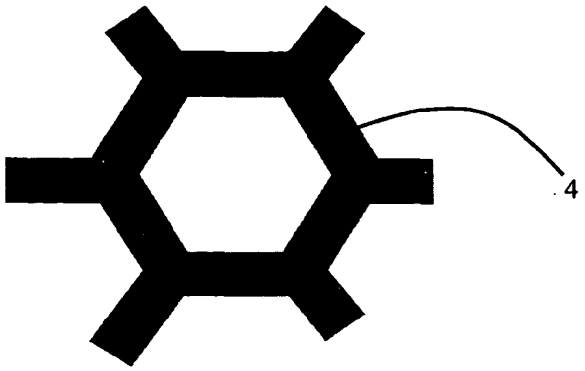

FIG. 2A (Prior Art)

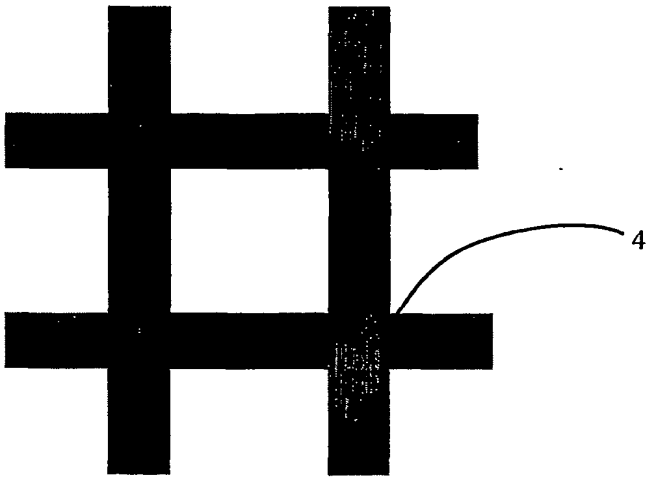

FIG. 2B (Prior Art)

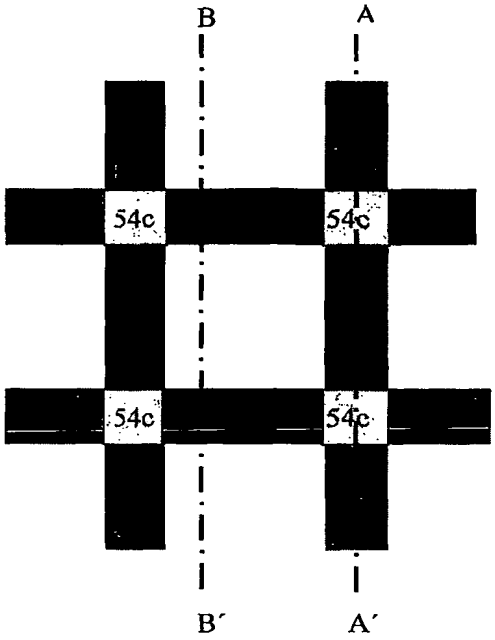

FIG. 3

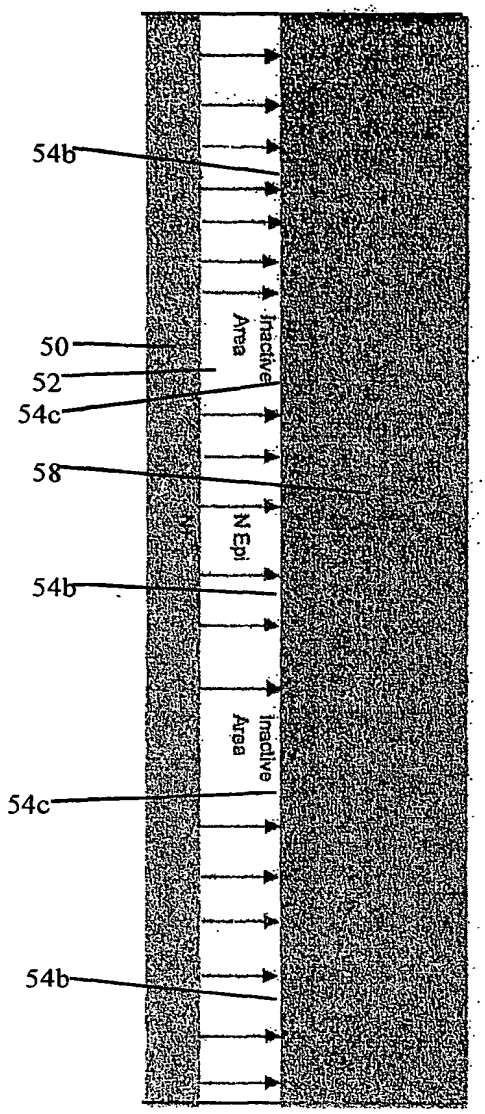
54b
50
52
54c
58
54b
54c
54b
Inactive Area
N Epi
Inactive Area

Fig. 4A

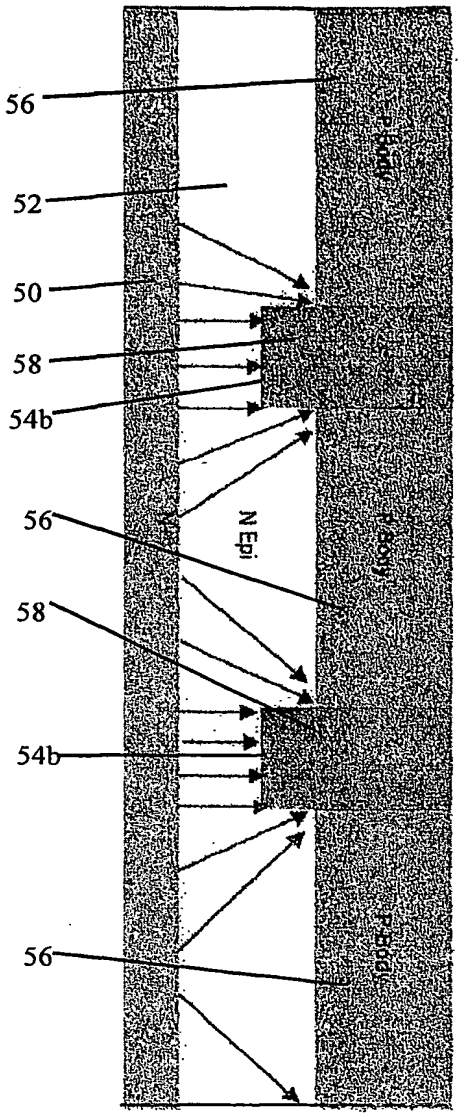
56
52
50
58
54b
56
58
54b
56
N Epi
P Body
P Body

Fig. 4B

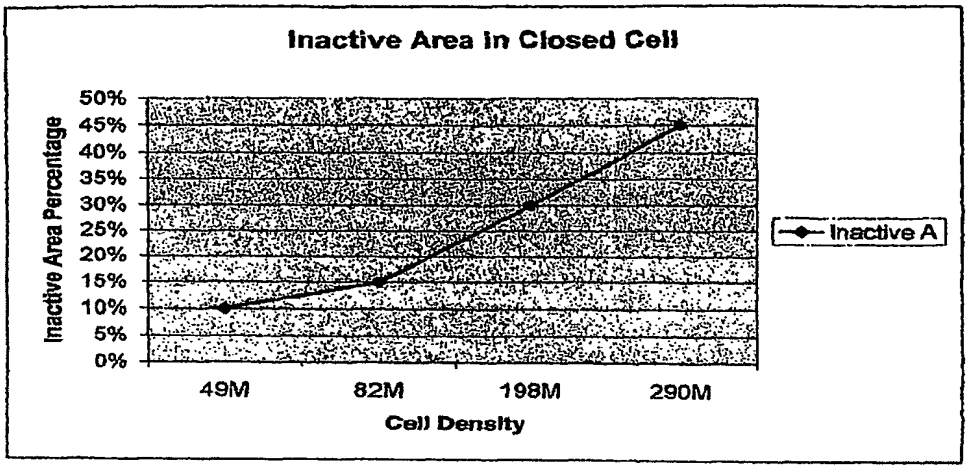
Inactive Area in Closed Cell
Inactive Area Percentage
50%
45%
40%
35%
30%
25%
20%
15%
10%
5%
0%
49M
82M
198M
290M
Cell Density
Inactive A

FIG. 5

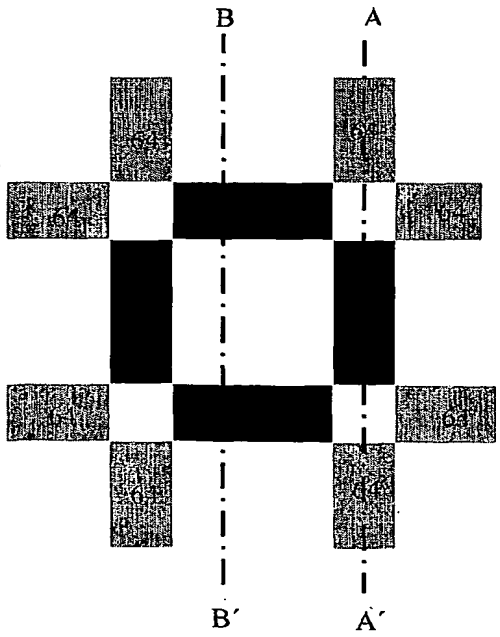
B
A
B'
A'

FIG. 6

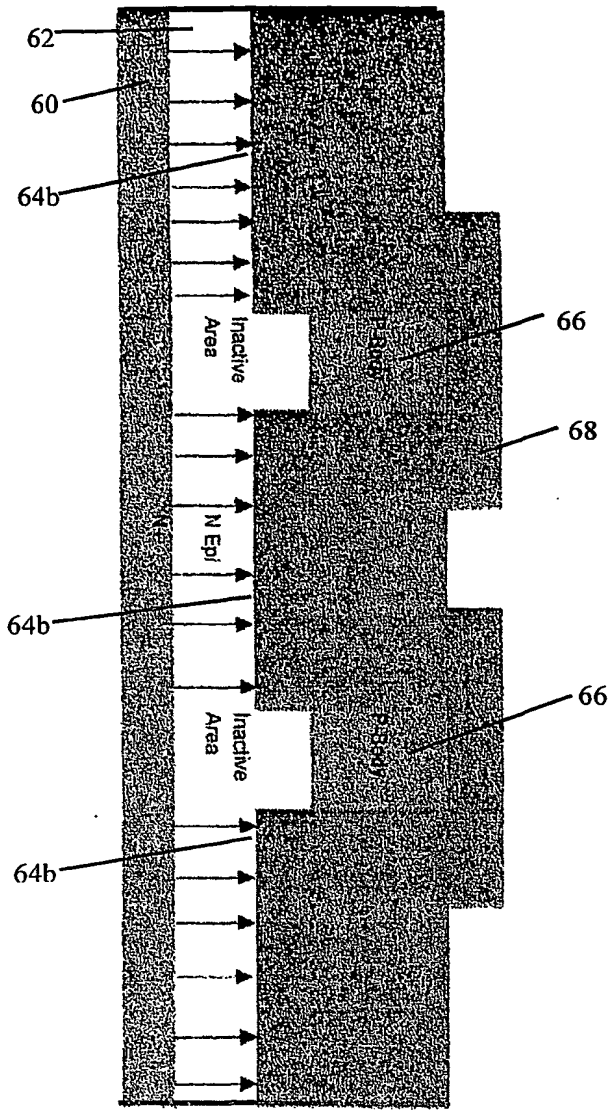
62
60
64b
Inactive Area
N Epi
P Body
66
68
64b
66
Inactive Area
64b

FIG. 7A

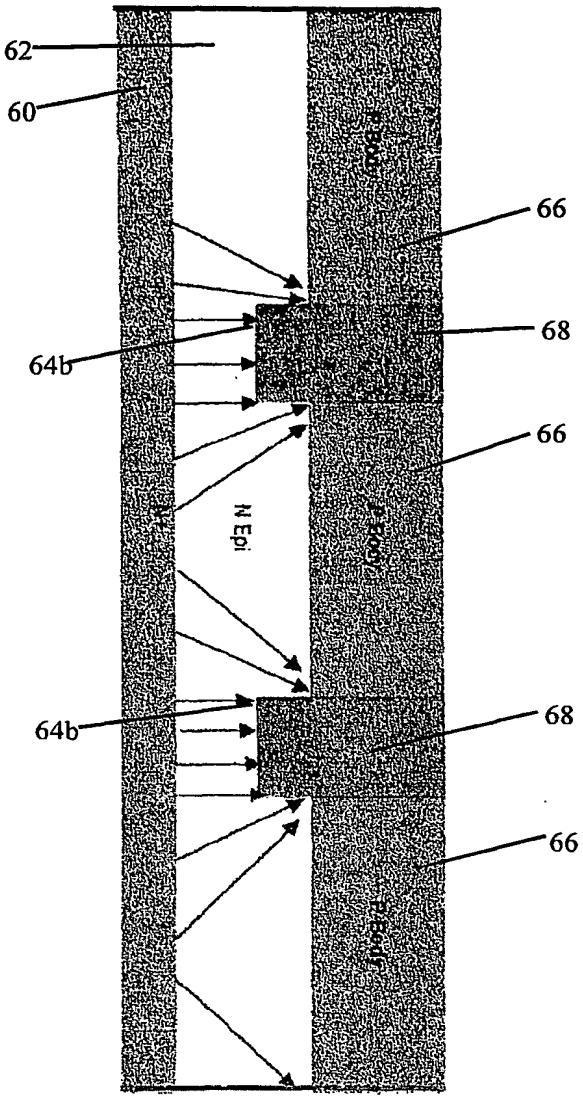
62
60
P Body
66
68
64b
66
N Epi
P Body
64b
68
66
P Body

FIG. 7B

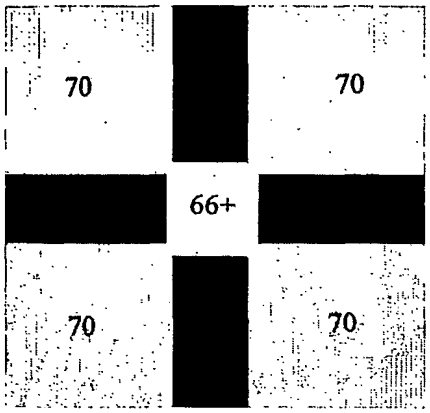

FIG. 8A

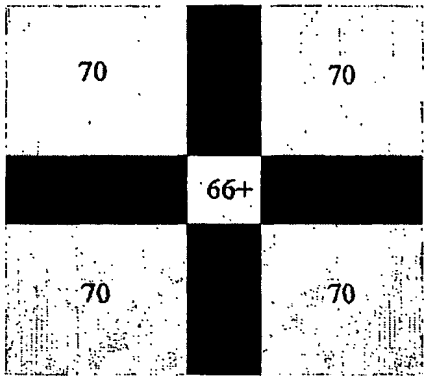

FIG. 8B

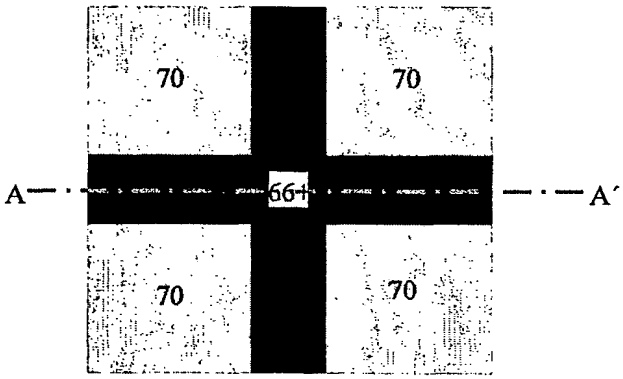

FIG. 8C

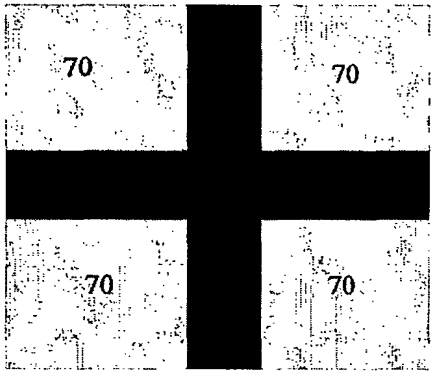

FIG. 8D (Prior Art)

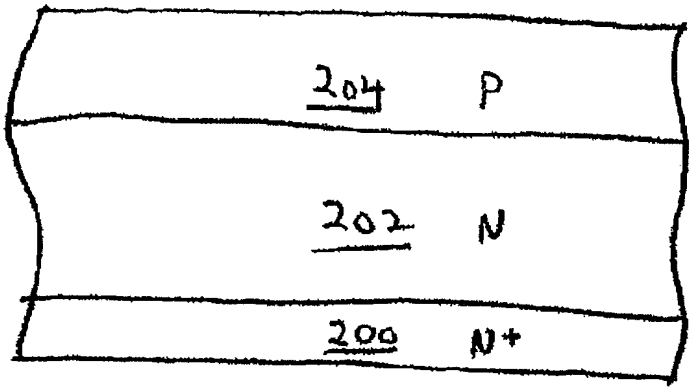

FIG. 9A

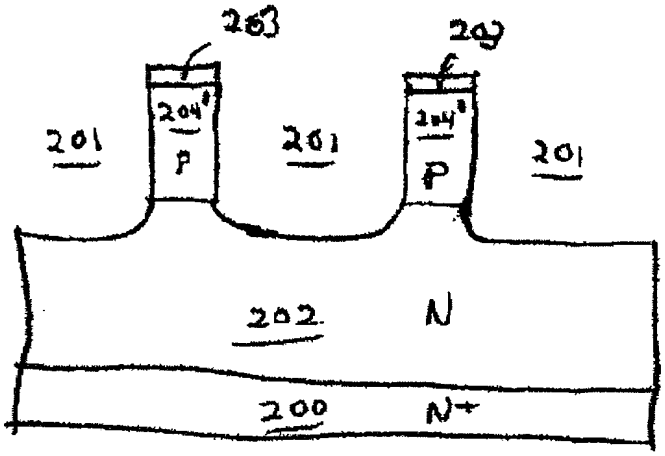

FIG. 9B

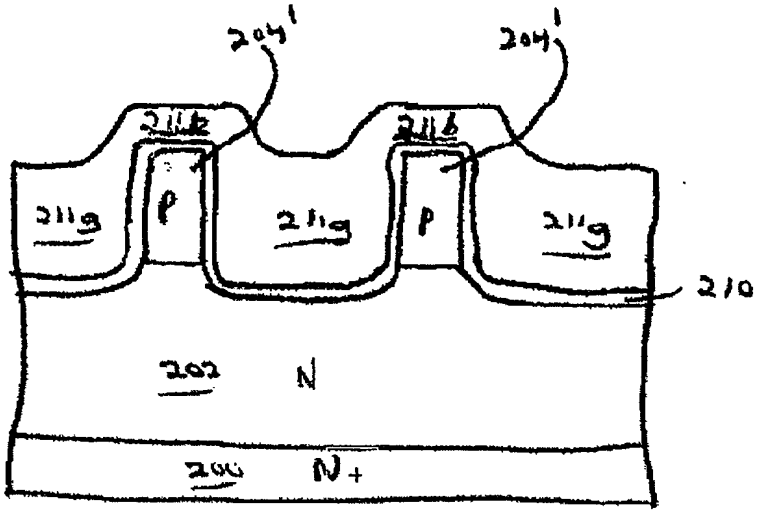
204'
204'
216
216
211g
P
211g
P
211g
210
202 N
200 N+

FIG. 9C

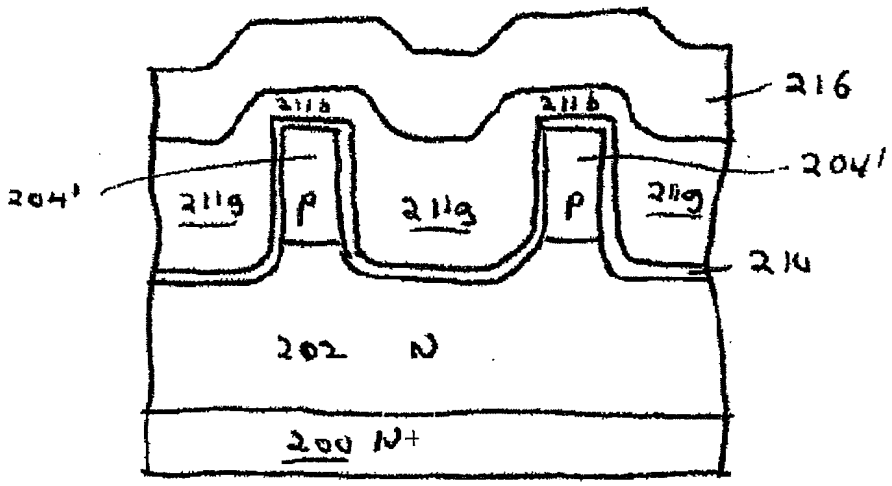
216
216
204'
204'
211g
P
211g
P
211g
214
202 N
200 N+

FIG. 9D

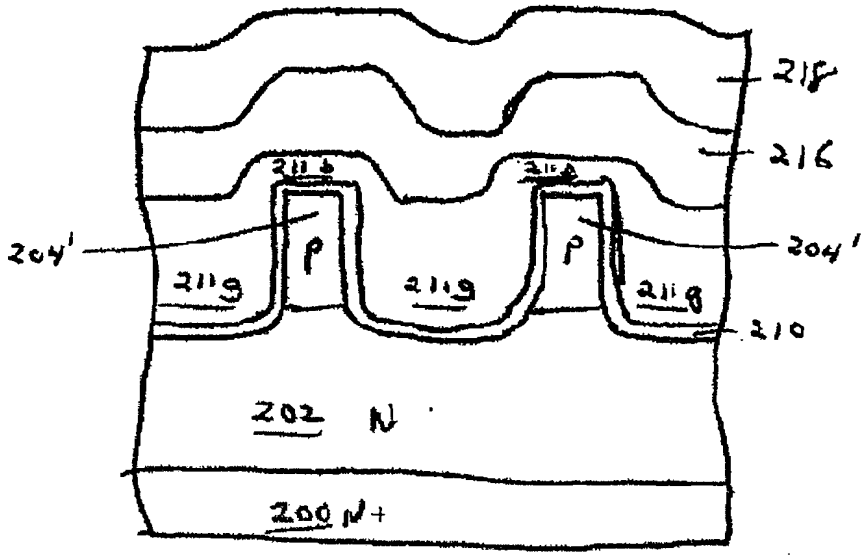

FIG. 9E

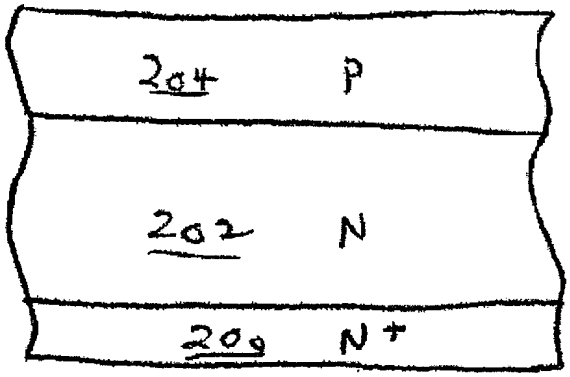

FIG. 10A

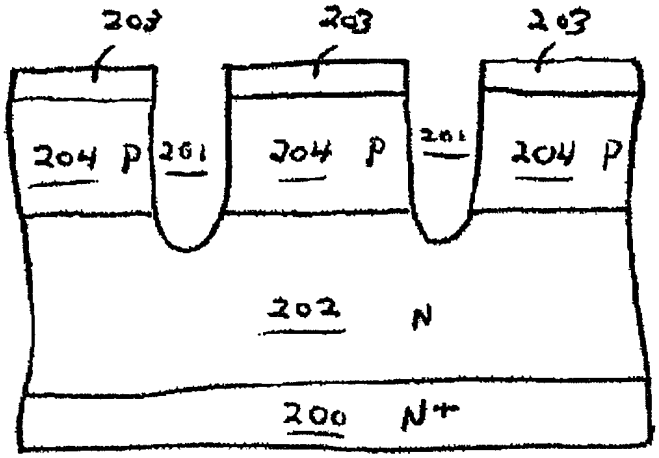

FIG. 10B

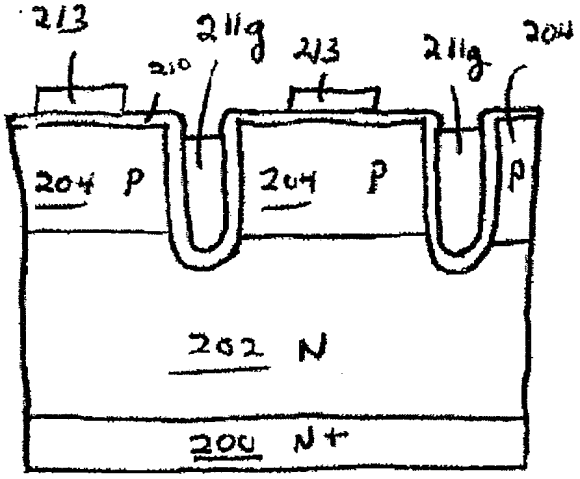

FIG. 10C

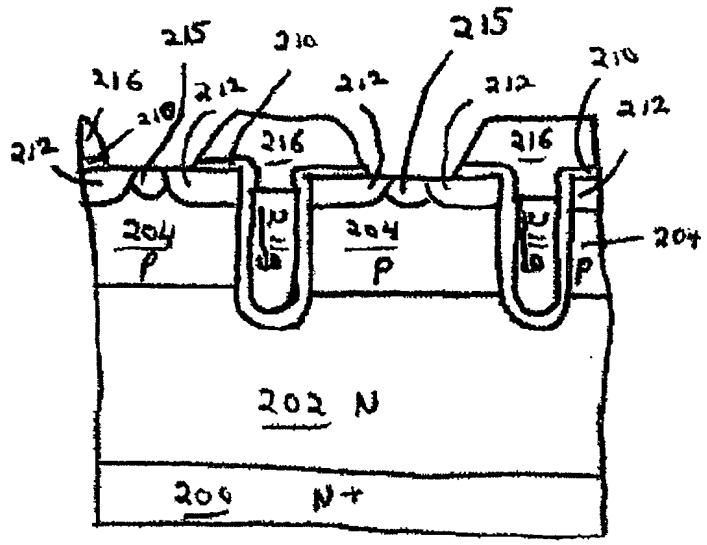

FIG. 10D

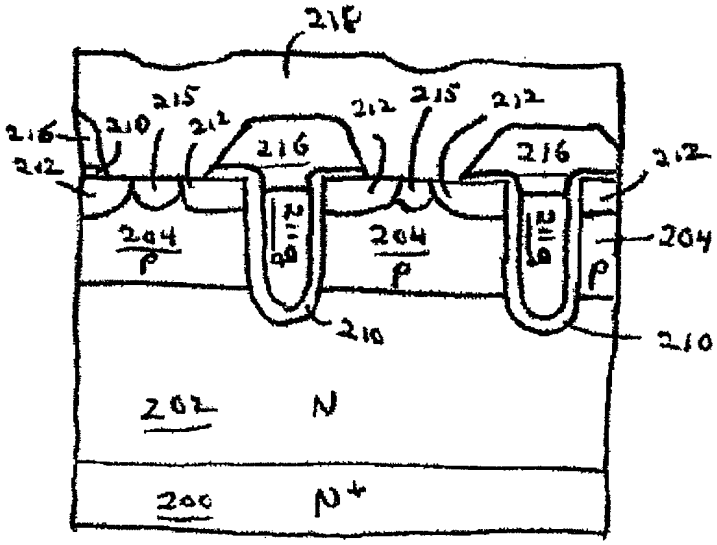

FIG. 10E

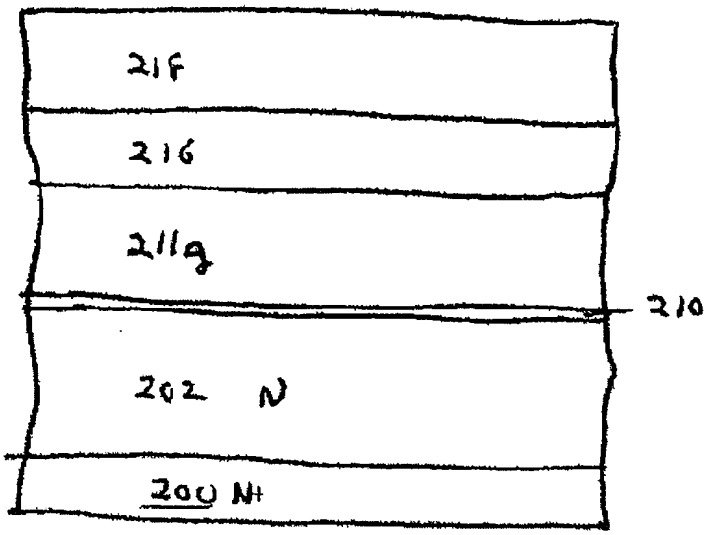

FIG. 11 (Prior Art)

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09/653,619 31 August 2000 (31.08.2000) US

(71) Applicant: GENERAL SEMICONDUCTOR, INC. [US/US]; 10 Melville Park Road, Melville, NY 11747-3113 (US).

(72) Inventors: HSHIEH, Fwu-Iuan; 20768 Sevilla Lane, Saratoga, CA 95070 (US). SO, Koon, Chong; 591 Woodview Terrace, Fremont, CA 94539 (US). TSUI, Yan Man; 4409 Drywood Court, Union City, CA 94587 (US).

(74) Agent: MAYER, Stuart, H.; Mayer Fortkort & Williams, PC, 2nd Floor, 251 North Avenue West, Westfield, NJ 07090 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

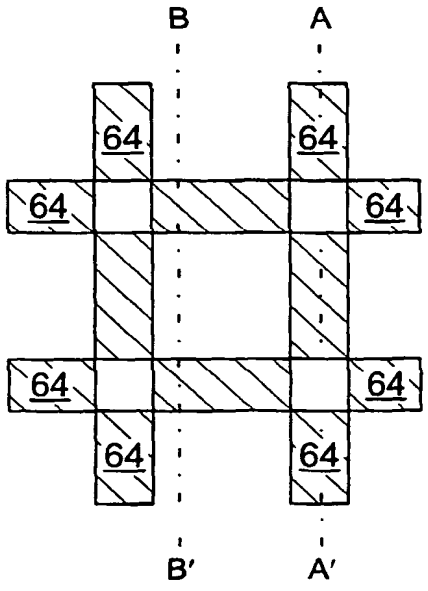
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
6 March 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: TRENCH MOSFET WITH STRUCTURE HAVING LOW GATE CHARGE



(57) Abstract: A trench MOSFET comprising: an epitaxial region of first conductivity type provided within a lower portion of an epitaxial layer disposed on a substrate, wherein the epitaxial region has a lower majority carrier concentration than the substrate;a region of second conductivity type provided within an upper portion of the epitaxial layer, trench segments in an upper surface of the epitaxial layer, wherein: i) the trench segments extend through said region and into the epitaxial region, ii) each trench segment is at least partially separated from an adjacent trench segment by a terminating region of the epitaxial layer, and iii) the trench segments define polygonal body regions within said region; conductive regions within the trench segments adjacent to the first insulating layer, wherein each of the conductive regions is connected to an adjacent conductive region by a connecting conductive region that bridges at least one of the terminating regions;

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/26819

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/10 H01L29/78 H01L29/06 H01L29/423

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 614 751 A (HSHIEH FWU-IUAN ET AL) 25 March 1997 (1997-03-25) column 5, line 12 - line 40; figure 5	1-22
X	EP 0 768 761 A (SILICONIX INC) 16 April 1997 (1997-04-16) figure 13	1,2, 4-11, 13-22
A	US 5 541 425 A (NISHIHARA HIDENORI) 30 July 1996 (1996-07-30) cited in the application the whole document	1-22
A	US 5 072 266 A (ROSSEN REBECCA ET AL) 10 December 1991 (1991-12-10) cited in the application figures 2B,8	3,12

-/--

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[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 October 2002	24/10/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Juhl, A

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/26819

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 866 931 A (ROSSEN REBECCA ET AL) 2 February 1999 (1999-02-02) cited in the application figure 7A	3,12
A	US 5 907 776 A (SO KOON CHONG ET AL) 25 May 1999 (1999-05-25) cited in the application figure 3	1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/26819

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
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US 5907776	A	25-05-1999	NONE		